CMOS Scaling, to what extent?

Anticipating increased difficulty in scaling CMOS technology for ICs, the microelectronics manufacturing industry will continue to deploy new technologies that provide additional functionality in ICs. Some new technologies will be evolutionary additions to current CMOS processes. Others will be revolutionary and will go well beyond the theoretical limits of CMOS scaling.

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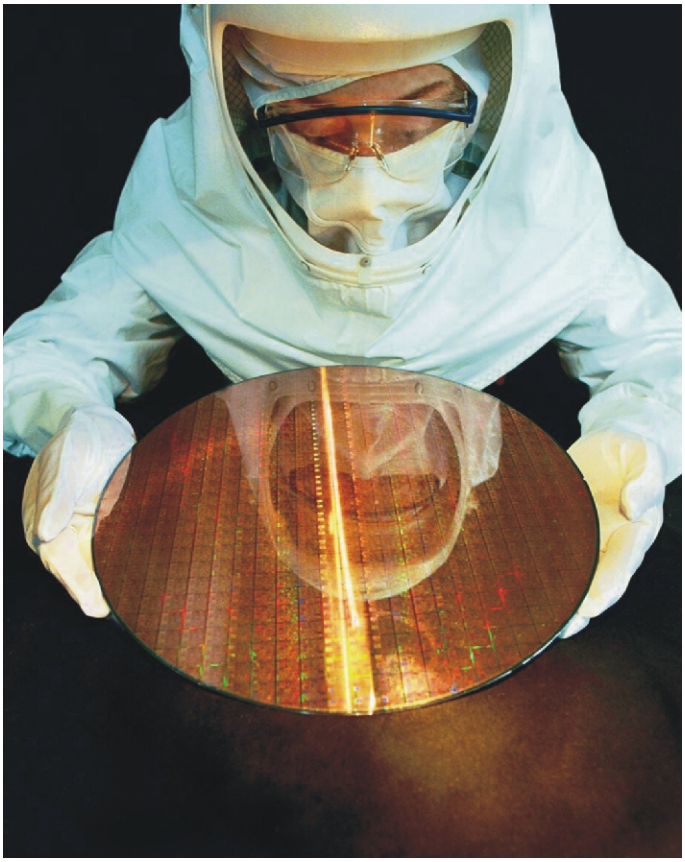
The tremendous growth in semiconductor technology has been based on the well-behaved Si-SiO2 system. In 1965, Gordon Moore, cofounder of Intel and arguably APL's most famous alumnus, saw the future. His prediction, now popularly known as Moore's Law, states that the number of transistors on a chip doubles approximately every 2 years. Up until now this "law" has been followed by



evolutionary progress of the basic technology. This progress has reached its limit. Major material modifications to the gate and drain regions of active devices will allow improvements in Si-based components to continue until 2020, but completely new concepts and technologies will be required to allow Moore's Law to hold after that. These technologies include graphene and carbon nanotube-based devices, single-electron transistors, spintronics, and quantum computing.

Scaling solid-state devices

The relentless drive in the semiconductor industry for smaller, faster and cheaper integrated circuits has brought the industry to the 32 nm technology node. The speed, computational power, and enhanced functionality of ICs based on this advanced technology promise to transform both our work and leisure environments. However the implementation of this technology has opened a Pandora's box of manufacturing issues as well as set the stage for a range of manufacturing challenges that require revolutionary new process methodologies as well as innovative, new equipment for the 22 nm and 15 nm nodes.

Scaling solid-state devices has the peculiar property of improving cost, performance, and power, which has historically given any company with the latest technology a large competitive advantage in the market. As a result, the microelectronics industry has driven transistor feature size scaling from 10 μm to ~30 nm during the past 40 years. During most of this time, scaling simply consisted of reducing the feature size. However, during certain periods, there were major changes as with the industry move from Si bipolar to

p-channel metal-oxidesemiconductor (MOS), then to n-channel MOS, and finally to complementary MOS (CMOS) planar transistors in the 1980s, which has remained the dominate technology for the past two decades. The big challenge going forward is that the end of planar CMOS transistor scaling is near as the transistor size approaches tens of nanometers. How the industry evolves after this limit is reached is unclear.

To address these challenges, present day research is focused on identifying new materials and devices that can augment and/or potentially replace the aging ~50-year-old Si transistor. Two approaches under investigation are: (1) nonclassical CMOS, which consists of new channel materials and/or multigate fully depleted device structures; and (2) alternatives to CMOS, such as spintronics, single electron devices, and molecular computing. While some of these non-Si research areas are important and will be successful in new applications and markets.

Challenges in CMOS technology node scaling

With assumption that Moore'e Law does not need an introduction we can dive directly into the issues faced by the semiconductor industry which has till now aggressively kept the Moore's law alive. The prediction still holds good and if it is up to companies like Intel and memory manufacturers it is expected to stay a valid prediction for some more time to come. But "transistor density doubling every two years" has not been a cake walk so far. There have been many road blocks which have been successfully been jumped over or worked around till now. The most significant among them would be reliability, noise, power and lithography. People sometimes assume lithography as the number one issue in moving to a smaller technology node, but the other factors mentioned above have equal relevance when considering the challenges of technology scaling. While lithography focuses on whether it would be possible to manufacture devices with smaller feature size, the others focus on how well such devices would work. As the technology scales to lower and lower nodes the above issues become more and more severe. Then why do semiconductor companies aggressively downscale technology. It is not just to keep the Moore's law alive. Moore's law being still valid is just a by product. The incentive comes from the fact the downscaling of technology leads to smaller

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dimensions of transistors, hence more denser circuits and resulting ideally in higher performance and lower dissipation of power. As the CMOS channel length is scaled down (analogous to CMOS technology node down scaling) the power voltage, threshold voltage and gate-oxide thickness are also reduced. Considering the electron thermal voltage being constant for a given temperature, the ratio of operating voltage to thermal voltage keeps shrinking. This leads to higher source-drain thermal current which is caused by thermal diffusion of electrons. Also the gate-oxide layer keeps reducing in thickness and for nodes 45nm and below it is just few atomic layer thick, hence quantum mechanical tunneling also give a sharp increase in gate leakage current. In short as we go towards smaller nodes the leakage current and current flowing through channel when gate voltage is below threshold voltage becomes a significant factor, and these currents are highly temperature sensitive and not dependant on power supply voltage.

Lithography is another significant point to consider when talking about technology scaling. The resolution of optical lithography has always been a concern, but it has outlasted it previous predicted doom by using better lenses, higher numerical aperture and shorter wavelength. Other techniques include change in the material optical mask to vary the phase of illuminating radiation. The resulting interference sharpens the image on wafer. But with these techniques too below 45nm scaling seems to hit the physical limits of optical lithography too.

Declared 22 nm CMOS technology

22nm Tri-Gate Transistor Technology declared by Intel continues Moore's Law. Intel demonstrates a 22nm microprocessor - codenamed "Ivy Bridge" - that will be the first high-volume chip to use 3-D Tri-Gate transistors.

The idea: Intel is always known for its advancements in microprocessor technology. Always on the pioneering front in this space, it's position in the microprocessor market remains at the top. Yet again, another invention has been done. This time, the world's first 3D transistors and

tri-gate technology will comprise Intel's 2011 processors.

Modified at a nano-scale, these transistors have lesser size and greater efficiency. Intel is the largest manufacturer of semiconductor chips. Most computers still run on its x86 series of microprocessors. Expanded as Integrated Electronics Corporation, Santa Clara-based Intel has come a long way since its inception in 1968.

Factbox:

Intel's 22nm Ivy Bridge processor	
Name	Ivy bridge
Developer	intel
Technology	22nm
Transistors used	Tri-Gate 3D
Transistor gate lengh	1nm

The making:

Intel has been using the 32 nanometre manufacturing process to make its transistors. Now these transistors will be made using the 22 nanometre manufacturing process. Making it smaller, and easier to pack more in less space, the transistors will increase in density per square area surface. Since the transistors use 3D tri-gate technology, they consume less power. Tri-Gate transistors will be used in high end servers to mobile devices. Code-named ''Ivy Bridge'', mass production of the transistors is expected before 2011.

At a recent event in San Francisco, Ivy Bridge was test-run on a notebook, desktop and a dual-core, single-core processor.

What's new:

Intel will now use the 22 nanometre manufacturing methodology for all future productions of its chips. The new chips will have enhanced processing capabilities, and will consume less electricity. Tri-Gate transistors have three conducting channels. They reside on the three sides of a vertical fin structure. This design ensures that transistors move away from traditional planar operation, and focus more towards reducing power leaks whilst functioning in lower voltage levels.

Future Predictions

The scaling of CMOS beyond 32nm tt's predicted that this may be the limit for current planar designs however, and it might be necessary to build the gates vertically on what are termed 'fins'. As 22nm

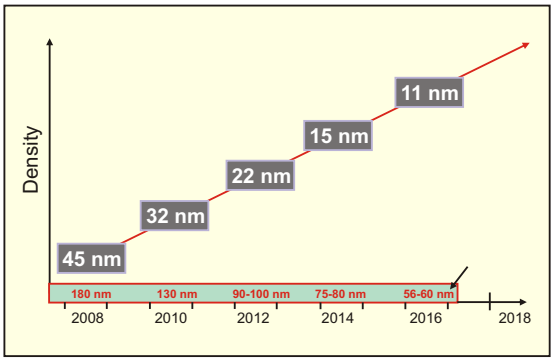

Fig. 2. CMOS scaling prediction to 11 nm node.

chips unveiled by Intel, the 16nm process is expected before 2018, although Intel reckons it will be there by 2013. New problems will arise, including excessive quantum tunnelling. This is where things get a bit weird as materials stop dancing to the rules of classical physics and Schrödinger's wave-equation pops up. Basically, it gets hard to stop the electrons breaching a barrier that's only a few nanometres thick no matter what material you use. This is also at the edge of commercial fabrication, nothing can currently be consistently and reliably made this small. Toshiba has built a prototype memory module with 15nm lines, but such sizes are still lab experiments. Next stop on the ladder down is the 11nm process, predicted for 2022 by the ITRS, although, again, Intel is more buoyant and talks of 2015. This is the expected limit of CMOS and may well mean silicon chips are no longer silicon. At this level dielectric thickness could be down to one atom, making it difficult to keep anything going where you want it to go. Figure 2 shows a possible CMOS technology roadmap through 11 nm node. However, even though transistor density continues to double every generation due to innovations in lithography, CMOS performance scaling is facing a formidable challenge (constrained by air cooling) due to a number of factors: increasing gate leakage current, rising active and passive power due to non-scaled voltage, band-to-band tunneling at high body doping levels, and insufficient source-drain doping for series resistance reduction.).

It is also expected to be the end for conventional photolithography, etching and polishing methods. After 11nm the roadmap has yet to be drawn, it appears that this is as far as current technologies can take us. Possible ways of making even smaller and more powerful chips include three dimensional arrays, using nanowires and tubes, single electron devices, spinbased.