# EDA Tools, What's New?

EDA is an important enabler to support fast product development cycles in the electronics industry. Chips with high functionality, multiple operating modes, low power consumption and extreme reliability—are pushing the manufacturing process to the limit. Requirements for enhancement of the EDA tools are growing with a similar speed as the improvements of the customers electronic products.

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There has been a drastic change in the market of electronics products from last few years. It's been years since consumers have bought products based on what was inside. From the EDA context, it is important to get a feel of the impact electronics has made in our lives. It is evident that Moore's Law will continue to hold and govern the EDA and the semiconductor industry for the next decade, maybe with small corrections – at least until we reach the limits of CMOS. Also, over the past few years, the number of new design starts has gradually declined, a trend that is likely to be more rapid in the coming years. At the same time, it is important to note that the designs are increasingly becoming more complex. As the scale and complexity of chip design increase, Electronic Design Automation (EDA) tools become much more sophisticated and are held to increasing standards of quality. New generation EDA tools must work correctly on a wider range of inputs, have more internal states, take more effort to develop, and offer fertile ground for programming mistakes. Ensuring quality of a commercial tool in realistic design flows requires rigorous simulation, non-trivial computational resources, accurate reporting of results and insightful analysis.

Traditional EDA tools for physical design and verification have reached limits due to greater manufacturing process variability and the growing size and complexity of designs that take advantage of the latest nanometer scaling. With the advent of new process technologies, the handoff between integrated circuit (IC) layout and manufacturing has changed from a simple check to a multi-step process where the layout design must be enhanced
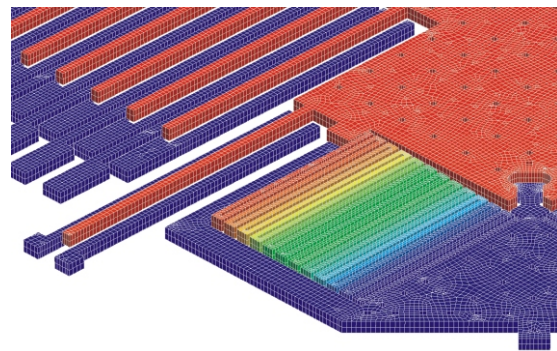
to ensure efficient manufacturing. This presents a host of challenges related to manufacturing process effects, photolithography, data volumes, and achieving a cost-effective yield of finished chips from each wafer.

EDA Challenges

The EDA industry tracks the trends in the semiconductor industry which is constantly evolving to cater to the 130, 90, 65 and even 45-nm silicon geometries. The whole electronics industry depends on the efficiency of these EDA tools, which would ensure smaller, faster, cheaper and more intelligent next-generation electronic products.

The EDA tools industry faces a high degree of technical change as it follows the technologically advanced semiconductor industry. The EDA tool vendors need to meet the design requirements of the semiconductor industry. The continuous size reduction in ICs from micro- to nanoscale dimensions drives the need for advanced and innovative EDA technologies to design the ever-shrinking devices.

The future trends indicate that devices may no longer be CMOS and newer ones based on the

likes of carbon nano-tubes, bio devices, and organic devices are likely to emerge. The same design methodologies that we use today will obviously be of no use. The EDA industry will need to put a razor sharp focus on creating flows, methodologies, and tools, to align with such emerging device technologies.

We conducted email Q&A with leading EDA companies to know EDA trends and best tools to satisfy latest demands along with their innovative tools list. We got responses from 2 EDA companies Cadence & MathWorks. Here are the views from Saugat Sen, Vice President – R&D, Cadence Design Systems (India) Pvt Ltd & Dr. Arun Mlupur, Industry Marketing Manager – Communications, Electronics, Semiconductors, MathWorks:

What are the latest important tools in your current portfolio?

Cadence: At Cadence, we continuously work towards maintaining our position as a leader in global electronic design innovation by developing and introducing world class technologies, services and IP. Recently Cadence announced the latest release of Cadence® Encounter® RTL-to-GDSII flow for high-performance and giga-scale designs, including those at the latest technology node, 20 nanometers. Developed in close collaboration with leading IP and foundry partners and customers, the new RTL-to-GDSII design, implementation and signoff flow enables more efficient development of SoCs, meeting and exceeding the power, performance and area demands of today's market requirements. The new RTL-to-GDSII flow builds on established Cadence successes, further advancing its technology leadership in power, performance, and area for the world's most advanced high-performance, low-power SoC designs.

Another recent significant technology release is Cadence System Development Suite that promises to cut system integration time by up to half for next-generation designs and provides a level of connection between hardware and software which not only enables the most efficient design methods possible, but redefines the whole system design process.

MathWorks: MathWorks recently announced HDL Coder generates portable and synthesizable VHDL and Verilog code directly from MATLAB® or Simulink® models. HDL Verifier supports FPGA-in-the-loop capabilities for testing and prototyping FPGA and ASIC designs and co-simulation with

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industry-leading HDL simulators. With HDL Coder and HDL Verifier, MathWorks is focused on and committed to streamlining both the implementation and verification aspects of FPGA and ASIC workflows.

According to you what is the best tool to satisfy current EDA customer need?

Cadence: Given the unique challenges facing our different customers - from consumer electronics to electronic medical devices - there is no one "silver bullet" technology that will satisfy all requirements. Design technologies and considerations for each vertical depend on the critical factors. For instance, in the consumer electronics industry, power, performance and area along with the user interface and applications are all critical care-abouts for chip designers. EDA technologies need to help designers meet these technology challenges, and also meet time-to-market windows and profitability goals. There are some overarching concerns which impact all customers equally. They are power, performance, mixed-signal design, verification, and advanced node design. In this regard, Cadence has been at the forefront of the technological innovations and has introduced technologies and flows that enable our customers design cutting-edge semiconductors.

MathWorks: It is not a stretch to say that the most important EDA tool in the world today is MATLAB. FPGA and ASIC designs today are math-heavy and

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algorithm-centric. MATLAB – as the de facto standard for algorithm exploration and system design – is the starting point for most designs that eventually get implemented on FPGAs and ASICs using traditional EDA tools. Engineers now have the ability to maintain their reference models in MATLAB or Simulink and automatically generate synthesizable HDL code at any time. The same reference models can also be used for design verification.

What are the enhancements that present-day EDA tools require to better design and design process?

Cadence: As end products become more and more sophisticated, the design complexity and challenges increase exponentially. Side by side, there is a forward march to design at progressively lower process nodes. In such a scenario, it is imperative that EDA companies constantly work on improving products and flows to help customers meet their aggressive objectives. Another trend that we are seeing is that systems companies are finding differentiation and value through the creative, innovative applications or "apps" that end consumers are demanding. This is true not only in the mobile handset world, where iPhone and Android are obvious examples, but anywhere there's a processor. The traditional approach to system development starts with the hardware, and

appends the software and the applications later.

MathWorks: At present, the key bottlenecks in EDA design are Design Abstraction or System-Level Design, Fixed-Point Design, and Verification. Design Abstraction and automatic code generation are closely coupled enhancements. Without code generation, any productivity benefits that engineers gain through system-level design are lost if they have to recode the designs manually. Design tools that offer the greatest advantages are those that directly address these bottlenecks, and connect productively with existing EDA tool flows.

What are the technological factors that will drive the growth and improvement of EDA tools?

Cadence: The move to advanced process nodes has heralded a number of challenges that require changes in the tools and methodologies. These challenges include increased timing and power variability, maximizing yield and manufacturability which involves complex layout rules, and incredibly large designs with massive amounts of IP. A major new challenge at 20nm is the requirement for extra masks (double patterning) to make existing lithography work at this advanced process node.

As with all technologies, we will need to continually upgrade technologies to keep up with changing consumer and market demands.

MathWorks: The enhancements we mentioned above are critical for the evolution and growth of next generation EDA tools. In fact, it is important to realize that engineering managers are tired of thinking about and worrying about tools. They have recognized that the next generation of math-heavy and algorithm-centric hardware can be efficiently designed only with well-integrated EDA flows – not individual tools. As a result, it is critical that the industry-standard algorithm and system-design and simulation environments be connected and well-integrated with established downstream EDA flows such as RTL simulation, synthesis, and place and route. Some of the key technology drivers that will enable next-generation EDA workflows are high-performance desktop computing – including multicore simulation platforms, FPGA-in-the-loop prototyping capabilities, and hardware/software co-design. These upgrades are logical next steps in the evolution of the hardware that engineers need to design and the tools and workflows they need to design that hardware.