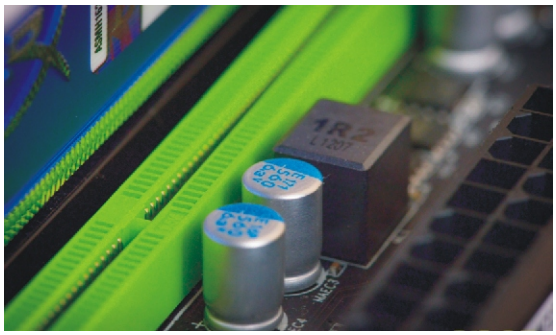
Causes of ESD on Semiconductor Advancements

Discussing new protective solutions from semicon players to tackle the issues.



ESD is a serious issue in solid state electronics, such as integrated circuits. Integrated circuits are made from semiconductor materials such as silicon and insulating materials such as silicon dioxide. Either of these materials can suffer permanent damage when subjected to high voltages; as a result, there are now a number of antistatic devices that help prevent static build up. ESD stands for ElectroStatic Discharge. A common explain for an ESD event is often described as the sudden transition of electric current that flows between two objects at different electrical potential, while in terms of electronics and semi conductors it refers to momentary unwanted currents that may cause damage to components and equipments.

EOS, Electrical Over Stress, is commonly the most frequently occurring failure mode in semiconductor devices of all types. ESD is actually a subset of the more general range of failures associated with EOS. However, EOS is generally associated with over-voltage and over-current stress of rather long time durations which usually associated with events that occur during normal circuit operation, screening or test conditions.

On the other hand, an ESD event counts as a short, fast and high amplitude pulses that are inevitable part of the day to day environment.

ESD is a miniature lightning bolt (spark) of charge that moves between two surfaces that have different potentials. It can occur only when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When a static charge moves, it becomes a current that damages or destroys gate oxide, metallization, and junctions.

ESD can occur in any one of four ways: a charged body can touch an integrated circuit (IC), a charged IC can touch a grounded surface, a charged machine can touch an IC, or an electrostatic field can induce a voltage across a dielectric sufficient to break it down.

What makes an ESD event important in electronics is that ESD is a relatively important cause of device (component) failure, whether in production line or at the user side. So it is vital to predict and prevent this type of failure as much as possible. There is

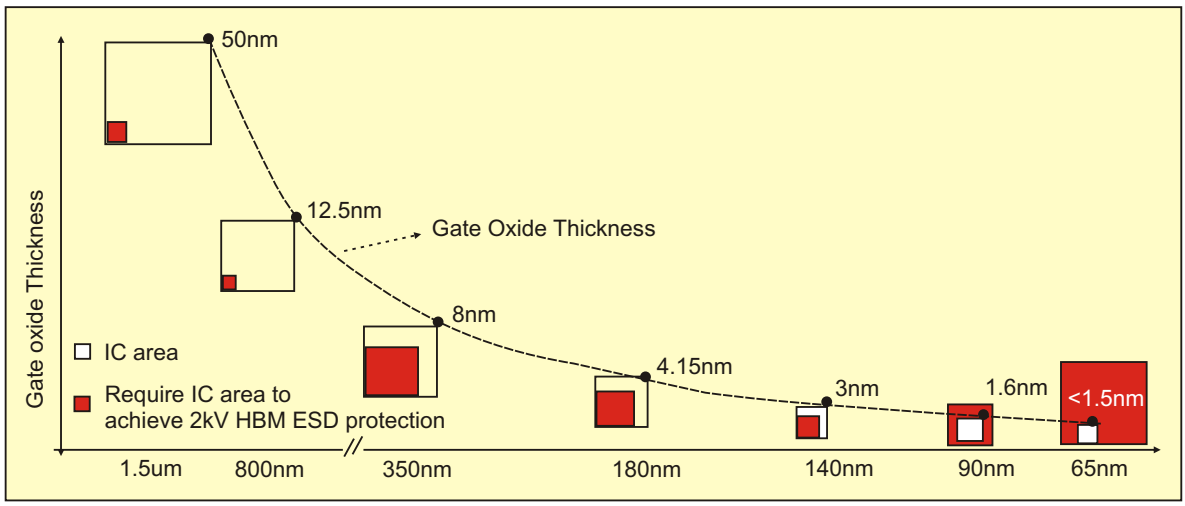


Fig. 1. ESD considerations for advanced CMOS ICs

growing interest in the effects of ESD on the performance of semiconductor ICs because of the impact ESD has on production yields and product quality.

ESD problems are increasing in the electronics industry because of the trends toward higher speed and smaller device sizes. ESD is a major consideration in the design and manufacture of ICs.

Impact of Moore's Law on ESD protection of advanced CMOS ICs

For 40 years the electronics industry has been able to successfully double the number of transistors on a circuit every two years. This path towards miniaturizations has become known as Moore's Law, named after visionary and Intel co-founder Gordon Moore.

The continuous trend of feature-size miniaturization has enabled semiconductor manufacturers over decades to improve chip performance, reduce power consumption, and drive cost down by squeezing billions of transistors into a single IC. Despite all obvious advantages, there is one major disadvantage in miniaturization of sub- circuits: integration of sufficiently robust ESD protection.

Figure 1 shows the reduction of the total IC area for various technology nodes. The red boxes within each of these ICs indicate schematically the required area to implement a minimum 2-kV ESD protection into the IC. [1]

With each technology node the relative area required for ESD protection increases. The reason is that ESD protection scales with the area of the diodes and these diodes can not be shrunk at the same scale as transistors required for logic functions. It is obvious that for very advanced technology nodes there is a physical and economical limitation to integrate robust enough ESD protection. Advanced ICs are optimized for power consumption and speed, not for ESD protection. An optimization for ESD protection would blow up the chip above any acceptable limit.

Curtis Wang, Senior Manager, Product Management, TE Circuit Protection –

"Today's consumer electronics and mobile devices are densely packed with processors, Application Specific Integrated Circuits (ASICs), and chipsets. In these components are millions of transistors and CMOS devices. As more and increasingly complex functions and applications are integrated into smart phones and mobile devices, more and smaller transistors must be packed into the limited space of the chipsets. Smaller transistors and CMOS devices are essential to high computing speeds, and the smaller these transistors and CMOS devices are, the more sensitive they are to damage caused by ESD events. In today's mobile applications, the processors and chipsets need to acquire input and transfer high speed data through ports in the mobile devices. These ports are frequently touched and held by humans. ESD strikes are directly conducted by the hand to the sensitive electronics and may cause damage if adequate ESD protection is not provided.

Stewart Logie, Vice President of Technology Development, Lattice Semiconductor –

"Two developments in semiconductor applications are causing exacerbated ESD effects that require attention from chip designers. First is the increasing use of high-speed interfaces at ever-increasing speed. Such interfaces operate at low voltages and need low capacitance ports. Low voltage transistors tend to be more fragile than traditional IO transistors and need additional ESD clamps to protect them. Those clamps must not add too much capacitance to the port or the speed will be degraded. Often, SCRs (Silicon Controlled Rectifier) are used with a voltage-tuned trigger to turn them on. These, and other snap-back devices, have the advantage of low leakage under normal operation, then channel the energy of the ESD pulse away from sensitive circuit elements. The second development is that with the increased prevalence of mobile equipment, users are plugging and unplugging equipment while systems are operational and in uncontrolled environments. This may

cause higher electrostatic voltages to be generated. Affected ICs may reside in active cables, peripheral devices and boards. The device designer must take care that plugging in peripherals does not cause the ESD protection clamps to latch up, but that the clamps turn on with low enough impedance to protect against the high ESD discharge.

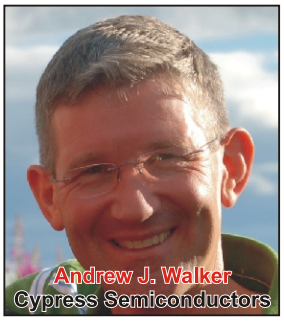
Wreeju Bhaumik, Analog Devices India (DSP Design Team) –

"The increasing usage of laptop computers, smart phones, and other electronic equipment create a situation where more users and more frequently might touch the input output connector pins during the connecting and disconnecting of cables or during normal usage. Integration of more and more inputs and outputs on our gadgets, higher current densities, smaller silicon geometries and limited space availability all of the above combined along with increasing usage of electronics devices leads to increase of voltage discharges. Protection of the electronics components during these high voltage discharges even though lasting for a fraction of a second is the key! ESD is typically the most common form of Electronic OverStress (EOS). Furthermore, the move to lower and lower geometries in semiconductor technology is increasing the impact of ESD as smaller geometries imply the following:

- Thinner gate oxides: Gate oxide breakdown voltages are critical in ESD and the thinner the gate oxide (i.e lower the geometry), the lower the oxide breakdown voltage under ESD stress.
- Lightly doped drains and silicided junctions: reduce the performance of the parasitic BJT that provides high current capability.
- Shallower junctions cause higher current densities during an ESD event.
- Pad pitch: The distance between I/O pads is decreasing at smaller geometries and reducing the area available for ESD protection circuits.

Andrew J. Walker, Tech Development Engineer Director - Senior at Cypress Semiconductors –

"The silicon chip business is a story of constant shrinking of devices often described by Moore's Law. As on-chip dimensions shrink and material layers used to make the chips thin down, ESD grows in importance as a potential failure mechanism. The main reason is that the voltages associated with ESD do not shrink. Therefore, the electric fields on-chip increase as we shrink resulting in a greater likelihood of failure.



Saugat Sen, Vice-President of SPB R&D. Cadence Design Systems (India) Pvt Ltd –

"Electrostatic discharge or ESD is caused by an abrupt flow of electricity between two components due to electric short, dielectric breakdown or friction. ESD is a critical issue in solid state electronics and semiconductors, and is quite common in integrated circuits. Integrated circuits are made up semiconductor and insulating materials such as silicon and silicon dioxide, and these materials when subjected to high voltage, can undergo permanent break down and damage. So, to prevent these phenomena, there are number of antistatic devices that protect and prevent the static build up.

ESD management during semiconductor manufacturing

Dealing with semiconductor ESD involves a seamless approach that includes building protection circuits into semiconductors during the design phase, taking various measures during the manufacturing phase, and taking measures from when semiconductors are finished until they are delivered to the customer (the distribution phase).

Curtis Wang, Senior Manager, Product Management, TE Circuit Protection –

"Chipsets integrate ESD protection devices which help protect the sensitive circuitry. These ESD devices, although many times larger than the transistors, are limited to a certain size based on available space in the die of the chipset. These small size ESD devices can only provide a low level

Main measures taken to deal with ESD during each phase	
Phase	**Main measure**
Design phase (measures taken during device and circuit design)	Design of an ESD protection circuit (design department, device development department) ESD immunity evaluation (design department, quality assurance department)
Manufacturing phase (measures taken during the wafer and assembly processes)	Measures to deal with ESD generated in the work environment (EPA*1) (process quality control department, facilities department, manufacturing department) Measures to deal with ESD generated by the human body (process control department, manufacturing department) Measures to deal with ESD generated by equipment, tools and jigs (facilities department)
Distribution phase (measures taken when packaging products and during transport)	Measures taken to deal with ESD generated during storage and in the work environment (packaging technology department, distribution management department) Measures taken to deal with ESD generated by packaging materials (packaging technology department, distribution management department)

of ESD protection. The ESD devices in the ASICs and chipset are often not robust enough to protect equipment from a high ESD strike level, and an 8kV contact discharge strike can make the chipset inoperable. Most engineers today have predominantly adopted the use of external ESD devices to protect the chipsets from damage cause by ESD contact discharge of up to 20kV.

Wreeju Bhaumik, Analog Devices India (DSP Design Team) –

"Engineers over the years have taken several steps to control and reduce the impact of the ESD issues.

1) The most common device used for ESD protection is the I/O transistor in something called "snapback". Under ESD stress, a positive feedback mechanism is activated that causes a parasitic npn BJT with much higher current capability to turn on and discharge the stress event.

2) An ESD implant (extra processing step) can be used to reduce the device breakdown voltage and create higher electric field in the snapback region leading to better ESD performance.

3) The drains of devices connected to I/O have a silicide blocking layer.

4) All I/O devices have primary ESD protection and on chip signals that traverse voltage domains are given secondary protection to prevent Field Induced Charged Device Model (FICDM) stress.

Please note that, Analog Design Inc. designs ICs that are relatively immune to dielectric damage by including proprietary ESD protection cells adjacent to bond pads and by including appropriate series resistors between the bond pads and the susceptible dielectric layers. The ESD protection cells are designed to turn-on extremely rapidly in response to an ESD event, thus clamping/limiting the voltage at the bond pad.

5) For low voltage (1.8V and below), power supply clamps operating in normal mode (not snapback) can be used, but their total widths are 4-5X that of snapback devices. If the connectivity to drain and source is symmetric, the large clamping device does not need ESD design rules, minimizing their area.

Analog Devices is committed to developing and releasing ICs that have high levels of robustness to electrical overstress (EOS) transients, including electrostatic discharge (ESD). All new products are tested to the Human Body Model (HBM) and the Field Induced Charged Device Model (FICDM) using stringent methods for this HBM and FICDM testing, consistent with the latest industry standards.

Beyond the semiconductor chip, additional off-chip protection is a must as system level ESD protection is the most important factor. Transient Voltage Suppressor (TVS) devices are the most common system (board) level ESD protection. These can be made small and pitch-matched to device pins, and placed very close to them. TVS devices can be used for I/O and supply pins as low as 1.8V. For I/O or supply voltages smaller than this, several diodes in series operating in forward bias to clamp the ESD event can be used.

Varistors have also been used, but these tend to have higher breakdown voltages which turn on at too high a voltage to protect the internal circuit without significant filtering (resistance/capacitance) between the varistor and ground. So these are not available in low voltage applications.

Zener diodes also are effective, similar to TVS devices. They have a sharp breakdown voltage and very low on-resistance. Their working voltage however is not as low as the newest TVS devices.

Furthermore, there is constant miniaturization on-going in this area to develop New ESD protection devices in Chip Scale Packaging e.g Back to back zener diode combinations in small chip scale footprint as an example. TVS, zener diode and varistor devices can be made in chip-scale packages today, so the package total size approximates the die. These are often bumped die.

Andrew J. Walker, Tech Development Engineer Director - Senior at Cypress Semiconductors –

"The increasing risk of ESD damage as we shrink the transistors on a chip means that our protection strategies against this threat become that more important. Protection can be divided into two main areas. First, we need to make sure that on-chip protection circuits do their job of limiting the impact of ESD zaps to our chips. Second, we need to reduce the chance that our chips experience such damaging zaps in the first place. This second part is associated with static charge control and reduction in environments where the chips will be handled both by humans and machines.

Besides reducing the chances of our chips experiencing damaging ESD events, we spend a good deal of time and effort in deriving and implementing on-chip protection circuits. These have two main functions, namely shunting ESD currents away from sensitive circuitry and clamping on-chip voltages safely below any damaging levels. Such shunting/clamping circuits are the result of experience and experiment. We make sure they do their job before we use them on a product by testing them out on test chips. We then apply the same kind of ESD zaps as they would experience in product qualification. Any deficiencies then are examined through failure analysis with fixes being put in place. The testing of ESD robustness both of test circuits and products is done by using industry standard zapping that can be classified into three main approaches, namely Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM). These can be seen as simulations of ESD events "in the wild" and are covered by various industry specifications that define the ESD pulses and the criteria for passing and failing.

Stewart Logie, Vice President of Technology Development, Lattice Semiconductor –

"At Lattice our device lab includes a test bench to measure ESD behavior and model it using our patented method. New clamps are built on test chips, which we then measure to build SPICE models for chip designers, who model ESD events and check for acceptable results before the chip is sent for fabrication.

Saugat Sen, Vice-President of SPB R&D, Cadence Design Systems (India) Pvt Ltd –

"Electrostatic discharge or ESD occurs when there is a charge imbalance. In any electrical component such as ICs, to balance potentials, the dissipating current tends to seek the lowest impedance path to ground. However, there are cases when ESD currents do not reach the ground and thus could burn the entire integrated circuit, with considerable amount of heat damage. A single instance does not disrupt equipment operation, but repeated instances over time can wreak havoc on the internal mechanisms of equipment. To counter the electro static build up, engineers designate Electrostatic Protective Areas (EPA) by taking precautionary measures such aslimiting or curtailing the presence of highly charged materials on ESD sensitive electronic components, and grounding all conductive materials.

In today's electronics/semiconductor industry where we are dealing with rapid advancements in chip designing, the amount of protection mechanisms available through traditional methods are just not enough and provides negligible protection. Also, these existing risks have adverse effects on high speed signaling interfaces which makes it difficult to meet regulatory standards. Moreover, with the reduced geometry of today's ICs, electronic components have become more vulnerable and exposed to ESD due to the reduction in fabrication geometry size. Since handheld devices are more prone to this problem, the proposed solutions should be cost sensitive to fulfill the needs of the consumer market.

References:

[1] - Dr. Tamim P. Sidiki, D. F. et al, "ESD protection for HDMI 1.3 interfaces", Network systems Designline, september 06, 2006,